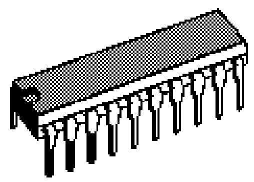
SGS-THOMSON MICROELECTRONICS

L4972A
L4972AD

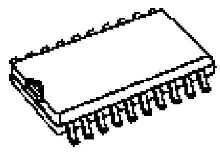
2A SWITCHING REGULATOR

- 2A OUTPUT CURRENT
- 5.1V TO 40V OUTPUT VOLTAGE RANGE
- 0 TO 90% DUTY CYCLE RANGE
- INTERNAL FEED-FORWARD LINE REG.
- INTERNAL CURRENT LIMITING
- PRECISE 5.1V ± 2% ON CHIP REFERENCE
- RESET AND POWER FAIL FUNCTIONS
- INPUT/OUTPUT SYNC PIN
- UNDER VOLTAGE LOCK OUT WITH HYSTERETIC TURN-ON
- PWM LATCH FOR SINGLE PULSE PER PERIOD
- VERY HIGH EFFICIENCY
- SWITCHING FREQUENCY UP TO 200KHz
- THERMAL SHUTDOWN
- CONTINUOUS MODE OPERATION

MULTIPOWER BCD TECHNOLOGY



POWERDIP
(16 + 2 + 2)



SO20

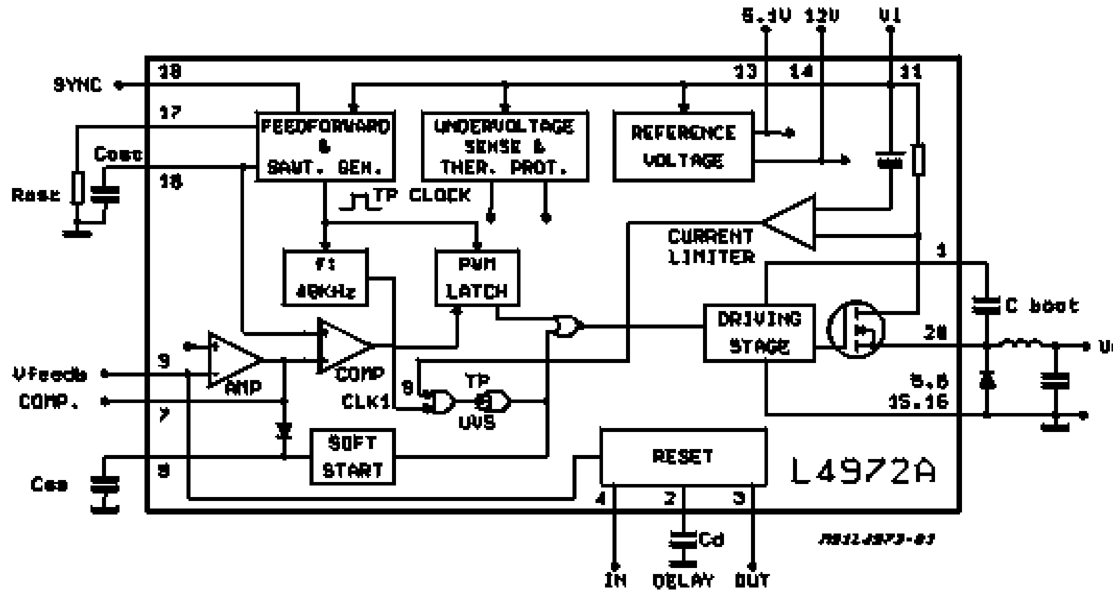
ORDERING NUMBERS : L4972A (Powerdip)
L4972AD (SO20)

DESCRIPTION

The L4972A is a stepdown monolithic power switching regulator delivering 2A at a voltage variable from 5.1 to 40V.

Realized with BCD mixed technology, the device uses a DMOS output transistor to obtain very high efficiency and very fast switching times. Features of the L4972A include reset and power fail for microprocessors, feed forward line regulation, soft start, limiting current and thermal protection. The device is mounted in a Powerdip 16 + 2 + 2 and SO20 large plastic packages and requires few external components. Efficient operation at switching frequencies up to 200KHz allows reduction in the size and cost of external filter component.

BLOCK DIAGRAM

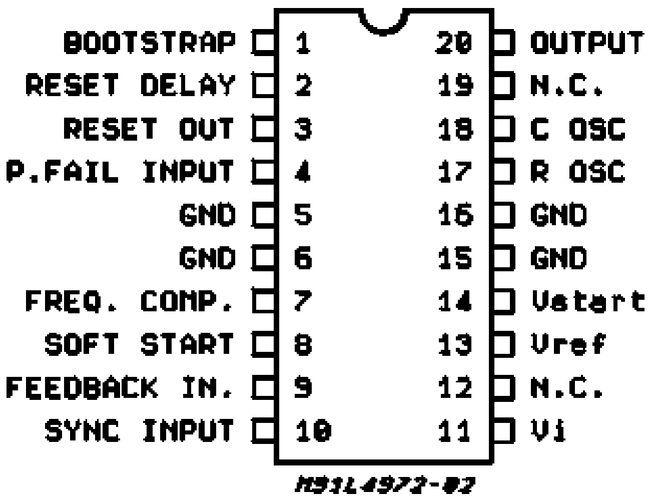


ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{11}	Input Voltage	55	V
V_{11}	Input Operating Voltage	50	V
V_{20}	Output DC Voltage Output Peak Voltage at t = 0.1μs f = 200khz	-1 -5	V V
I_{20}	Maximum Output Current	Internally Limited	
V_I	Boostrap Voltage Boostrap Operating Voltage	65 V_{11} + 15	V V
V_4, V_8	Input Voltage at Pins 4, 12	12	V
V_3	Reset Output Voltage	50	V
I_3	Reset Output Sink Current	50	mA
V_2, V_7, V_9, V_{10}	Input Voltage at Pin 2, 7, 9, 10	7	V
I_2	Reset Delay Sink Current	30	mA
I_7	Error Amplifier Output Sink Current	1	A
I_8	Soft Start Sink Current	30	mA
P_{tot}	Total Power Dissipation at T_{PINS} ≤ 90°C at T_{amb} = 70°C (No copper area on PCB)	5 / 3.75(*) 1.3/1 (*)	W W
T_J, T_{stg}	Junction and Storage Temperature	-40 to 150	°C

(*) SO-20

PIN CONNECTION (top view)



THERMAL DATA

Symbol	Parameter		Powerdip	SO-20
$R_{th\ j\text{-}pins}$	Thermal Resistance Junction-Pins	max	12°C/W	16°C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	max	60°C/W	80°C/W

PIN FUNCTIONS

N°	Name	Function
1	BOOTSTRAP	A C_{boot} capacitor connected between this terminal and the output allows to drive properly the internal D-MOS transistor.
2	RESET DELAY	A C_d capacitor connected between this terminal and ground determines the reset signal delay time.
3	RESET OUT	Open Collector Reset/power Fail Signal Output. This output is high when the supply and the output voltages are safe.
4	RESET INPUT	Input of Power Fail Circuit. The threshold is 5.1V. It may be connected via a divider to the input for power fail function. It must be connected to the pin 14 an external 30KΩ resistor when power fail signal not required.
5, 6 15, 16	GROUND	Common Ground Terminal
7	FREQUENCY COMPENSATION	A series RC network connected between this terminal and ground determines the regulation loop gain characteristics.
8	SOFT START	Soft Start Time Constant. A capacitor is connected between thi sterminal and ground to define the soft start time constant.
9	FEEDBACK INPUT	The Feedback Terminal of the Regulation Loop. The output is connected directly to this terminal for 5.1V operation; It is connected via a divider for higher voltages.
10	SYNC INPUT	Multiple L4972A's are synchronized by connecting pin 10 inputs together or via an external syncr. pulse.
11	SUPPLY VOLTAGE	Unregulated Input Voltage.
12, 19	N.C.	Not Connected.
13	V_{ref}	5.1V V_{ref} Device Reference Voltage.
14	V_{start}	Internal Start-up Circuit to Drive the Power Stage.
17	OSCILLATOR	R_{osc}. External resistor connected to ground determines the constant charging current of C_{osc}.
18	OSCILLATOR	C_{osc}. External capacitor connected to ground determines (with R_{osc}) the switching frequency.
20	OUTPUT	Regulator Output.

CIRCUIT OPERATION

The L4972A is a 2A monolithic stepdown switching regulator working in continuous mode realized in the new BCD Technology. This technology allows the integration of isolated vertical DMOS power transistors plus mixed CMOS/Bipolar transistors.

The device can deliver 2A at an output voltage adjustable from 5.1V to 40V and contains diagnostic and control functions that make it particularly suitable for microprocessor based systems.

BLOCK DIAGRAM

The block diagram shows the DMOS power transistors and the PWM control loop. Integrated functions include a reference voltage trimmed to 5.1V ± 2%, soft start, undervoltage lockout, oscillator with feedforward control, pulse by pulse current limit, thermal shutdown and finally the reset and power fail circuit. The reset and power fail circuit provides an output signal for a microprocessor indicating the status of the system.

Device turn on is around 11V with a typical 1V hysterysis, this threshold porvides a correct voltage for the driving stage of the DMOS gate and the hysterysis prevents instabilities.

An external bootstrap capacitor charge to 12V by an internal voltage reference is needed to provide correct gate drive to the power DMOS. The driving circuit is able to source and sink peak currents of around 0.5A to the gate of the DMOS transistor. A typical switching time of the current in the DMOS transistor is 50ns. Due to the fast commutation switching frequencies up to 200kHz are possible.

The PWM control loop consists of a sawtooth oscillator, error amplifier, comparator, latch and the output stage. An error signal is produced by comparing the output voltage with the precise 5.1V ± 2% on chip reference. This error signal is then compared with the sawtooth oscillator in order to generate frixed frequency pulse width modulated drive for the output stage. A PWM latch is included to eliminate multiple pulsing within a period even in noisy environments.

The gain and stability of the loop can be adjusted by an external RC network connected to the output of the error amplifier. A voltage feedforward control has been added to the oscillator, this maintains superior line regulation over a wide input voltage range. Closing the loop directly gives an output vol-tage of 5.1V, higher voltages are obtained by inserting a voltage divider.

At turn on, output overcurrents are prevented by the soft start function (fig. 2). The error amplifier is initially clamped by an external capacitor, Css, and allowed to rise linearly under the charge of an internal constant current source.

Output overload protection is provided by a current limit circuit. The load current is sensed by a internal metal resistor connected to a comparator. When the load current exceeds a preset threshold, the output of the comparator sets a flip flop which turns off the power DMOS. The next clock pulse, from an internal 40kHz oscillator, will reset the flip flop and the power DMOS will again conduct. This current protection method, ensures a constant current output when the system is overloaded or short circuited and limits the switching frequency, in this condition, to 40kHz. The Reset and Power fail circuit (fig. 4), generates an output signal when the supply voltage exceeds a threshold programmed by an external voltage divider. The reset signal, is generated with a delay time programmed by a external capacitor on the delay pin. When the supply voltage falls below the threshold or the output voltage goes below 5V, the reset output goes low immediately. The reset output is an open drain.

Fig. 4A shows the case when the supply voltage is higher than the threshold, but the output voltage is not yet 5V.

Fig. 4B shows the case when the output is 5.1V, but the supply voltage is not yet higher than the fixed threshold.

The thermal protection disables circuit operation when the junction temperature reaches about 150°C and has a hysterysis to prevent unstable conditions.

Figure 1 : Feedforward Waveform.

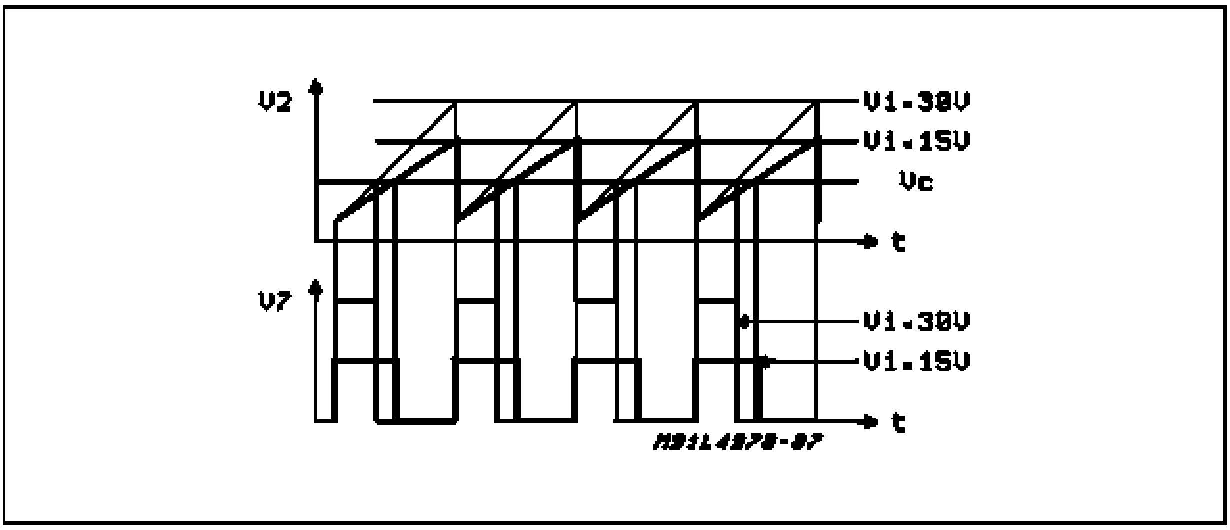


Figure 2 : Soft Start Function.

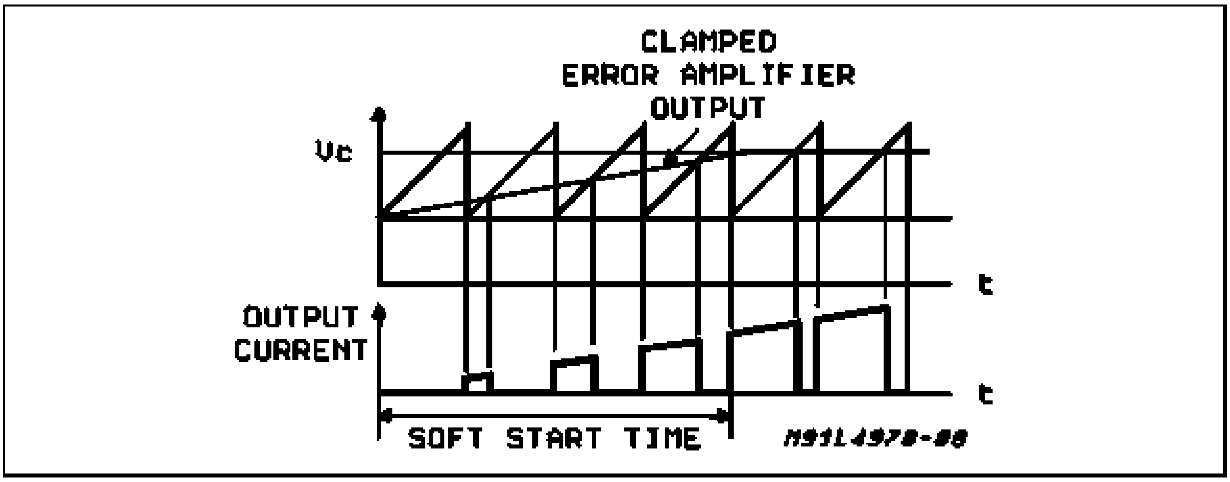


Figure 3 : Limiting Current Function.

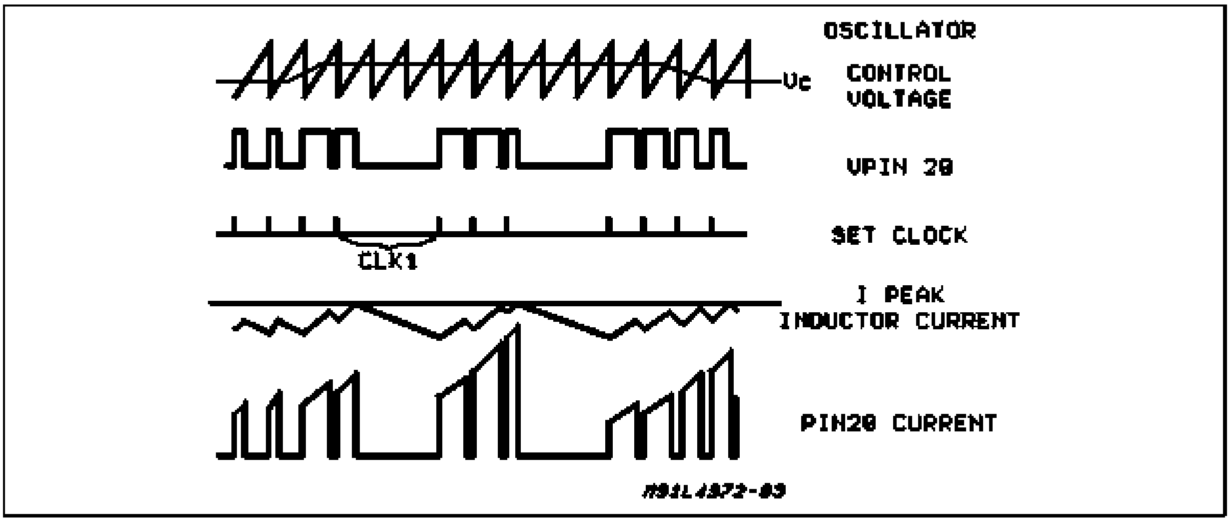
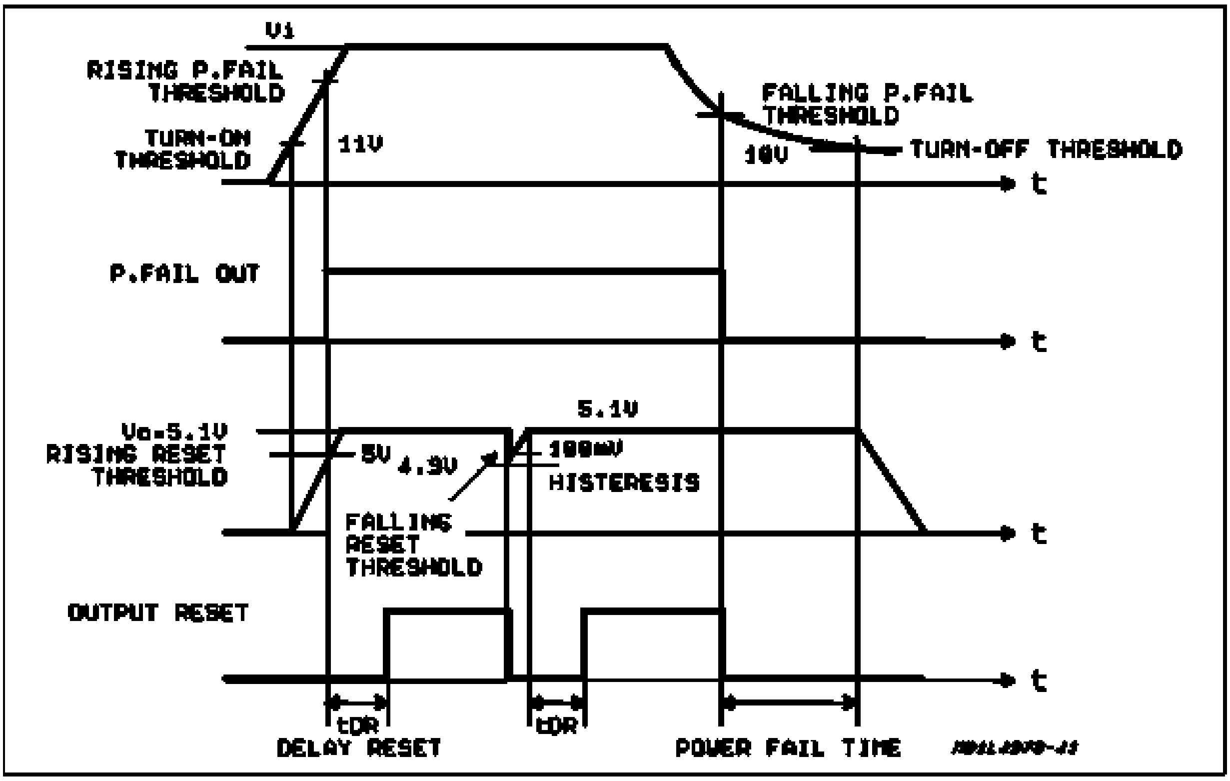
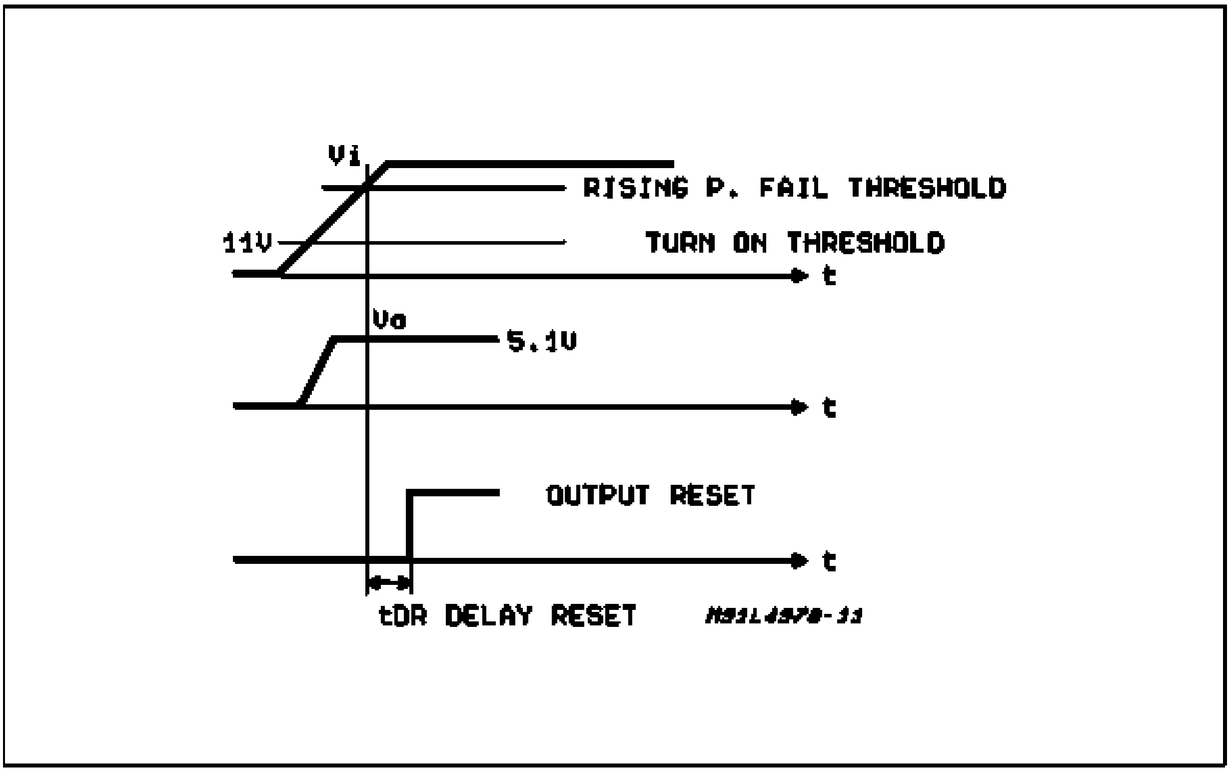


Figure 4 : Reset and Power Fail Functions.

A



B



ELECTRICAL CHARACTERISTICS (refer to the test circuit, T_J = 25°C, V_i = 35V, R_4 = 30KΩ, C_9 = 2.7nF, f_{SW} = 100KHz typ, unless otherwise specified)

DYNAMIC CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
V_i	Input Volt. Range (pin 11)	V_o = V_{ref} to 40V I_o = 2A (**)	15		50	V	5
V_o	Output Voltage	V_i =15V to 50V I_o = 1A; V_o = V_{ref}	5	5.1	5.2	V	5
ΔV_o	Line Regulation	V_i = 15V to 50V I_o = 0.5A; V_o = V_{ref}		12	30	mV	
ΔV_o	Load Regulation	V_o = V_{ref} I_o = 0.5A to 2A		7	20	mV	
V_d	Dropout Voltage between Pin 11 and 20	I_o = 2A		0.25	0.4	V	
I_{20L}	Max Limiting Current	V_i = 15V to 50V V_o = V_{ref} to 40V	2.5	2.8	3.5	A	
η	Efficiency (*)	I_o = 2A, f = 100KHz V_o = V_{ref} V_o = 12V	 75	 85 90		 % %	
SVR	Supply Voltage Ripple Rejection	V_i = 2VRMS; I_o = 1A f = 100Hz; V_o = V_{ref}	56	60		dB	5
f	Switching Frequency		90	100	110	KHz	5
$\Delta f/\Delta V_i$	Voltage Stability of Switching Frequency	V_i = 15V to 45V		2	6	%	5
$\Delta f/T_j$	Temperature Stability of Switching Frequency	T_j = 0 to 125°C		1		%	5
f_{max}	Maximum Operating Switching Frequency	V_o = V_{ref} R_4 = 15KΩ I_o = 2A C_9 = 2.2nF	200			KHz	5

(*) Only for DIP version (**) Pulse testing with a low duty cycle

V_{ref} SECTION (pin 13)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
V_{13}	Reference Voltage		5	5.1	5.2	V	7
ΔV_{13}	Line Regulation	V_i = 15V to 50V		10	25	mV	7
ΔV_{13}	Load Regulation	I_{13} = 0 to 1mA		20	40	mV	7
$\frac{\Delta V_{13}}{\Delta T}$	Average Temperature Coefficient Reference Voltage	T_j = 0°C to 125°C		0.4		mV/°C	7
$I_{13\,short}$	Short Circuit Current Limit	V_{13} = 0		70		mA	7

V_{START} SECTION (pin 15)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
V_{14}	Reference Voltage		11.4	12	12.6	V	7
ΔV_{14}	Line Regulation	V_i = 15 to 50V		0.6	1.4	V	7
ΔV_{14}	Load Regulation	I_{14} = 0 to 1mA		50	200	mV	7
$I_{14\,short}$	Short Circuit Current Limit	V_{15} = 0V		80		mA	7

ELECTRICAL CHARACTERISTICS (continued)

DC CHARACTERISTICS

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
V_{11on}	Turn-on Threshold		10	11	12	V	7A
$V_{11\ Hyst}$	Turn-off Hysteresys			1		V	7A
I_{11Q}	Quiescent Current	$V_8 = 0$; S1 = D		13	19	mA	7A
I_{11OQ}	Operating Supply Current	$V_8 = 0$; S1 = B; S2 = B		16	23	mA	7A
I_{20L}	Out Leak Current	$V_i = 55V$; S3 = A; $V_8 = 0$			2	mA	7A

SOFT START (pin 8)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
I_8	Soft Start Source Current	$V_8 = 3V$; $V_9 = 0V$	80	115	150	µA	7B
V_8	Output Saturation Voltage	$I_8 = 20mA$; $V_{11} = 10V$ $I_8 = 200\mu A$; $V_{11} = 10V$			1 0.7	V V	7B 7B

ERROR AMPLIFIER

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
V_{7H}	High Level Out Voltage	$I_7 = 100\mu A$; S1 = C $V_9 = 4.7V$	6			V	7C
V_{7L}	Low Level Out Voltage	$I_7 = 100\mu A$; S1 = C $V_9 = 5.3V$;			1.2	V	7C
I_{7H}	Source Output Current	$V_7 = 1V$; $V_7 = 4.7V$	100	150		µA	7C
$-I_{7L}$	Sink Output Current	$V_7 = 6V$; $V_9 = 5.3V$	100	150		µA	7C
I_9	Input Bias Current	S1 = B; $R_S = 10K\Omega$		0.4	3	µA	7C
G_V	DC Open Loop Gain	S1 = A; $R_S = 10\Omega$	60			dB	7C
SVR	Supply Voltage Rejection	$15 < V_i < 50V$	60	80		dB	7C
V_{OS}	Input Offset Voltage	$R_S = 50\Omega$ S1 = A		2	10	mV	7C

RAMP GENERATOR (pin 18)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
V_{18}	Ramp Valley	S1 = B; S2 = B	1.2	1.5		V	7A
V_{18}	Ramp Peak	S1 = B, S2 = B; $V_i = 15V$ S1 = B, S2 = B; $V_i = 45V$		2.5 5.5		V V	7A 7A
I_{18}	Min. Ramp Current	S1 = A; $I_{17} = 100\mu A$		270	300	µA	7A
I_{18}	Max. Ramp Current	S1 = A; $I_{17} = 1mA$	2.4	2.7		mA	7A

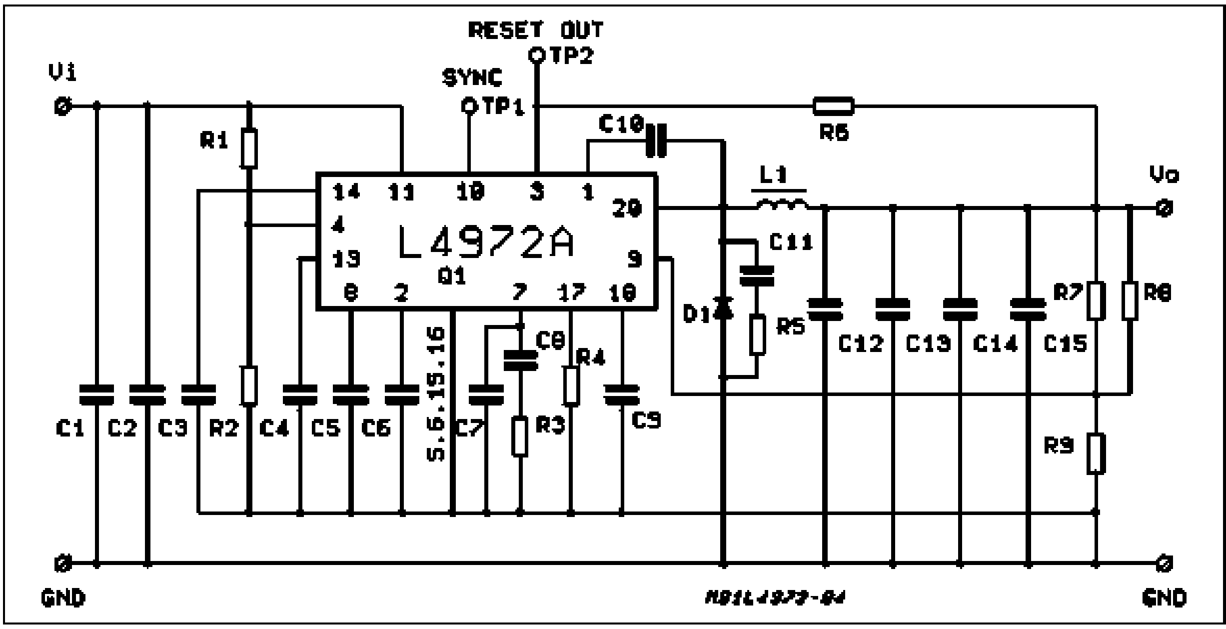
SYNC FUNCTION (pin 10)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Fig.
V_{10}	Low Input Voltage	$V_i = 15V$ to 50V; $V_8 = 0$; S1 = B; S2 = B; S4 = B	–0.3		0.9	V	7A
V_{10}	High Input voltage	V8 = 0; S1 = B; S2 = B; S4 = B	2.5		5.5	V	7A
I_{10L}	Sync Input Current with Low Input Voltage	$V_{10} = V_{18} = 0.9V$; S4 = B; S1 = B; S2 = B			0.4	mA	7A
I_{10H}	Input Current with High Input Voltage	$V_{10} = 2.5V$			1.5	mA	7A
V_{10}	Output Amplitude		4	5		V	–
t_W	Output Pulse Width	$V_{thr} = 2.5V$	0.3	0.5	0.8	µs	–

ELECTRICAL CHARACTERISTICS (continued)

RESET AND POWER FAIL FUNCTIONS

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
V_{9R}	Rising Thereshold Voltage (pin 9)	V_i = 15 to 50V V_4 = 5.3V	V_{ref} -130	V_{ref} -100	V_{ref} -80	V mV	7D
V_{9F}	Falling Thereshold Voltage (pin 9)	Vi = 15 to 50V V_4 = 5.3V	4.77	Vref -200	V_{ref} -160	V mV	7D
V_{2H}	Delay High Threshold Volt.	Vi = 15 to 50V V_4 = 5.3V $V_9 = V_{13}$	4.95	5.1	5.25	V	7D
V_{2L}	Delay Low Threshold Volt.	Vi = 15 to 50V V_4 = 4.7V $V_9 = V_{13}$	1	1.1	1.2	V	7D
I_{2SO}	Delay Source Current	V_4 = 5.3V; V_2 = 3V	30	60	80	µA	7D
I_{2SI}	Delay Source Sink Current	V_4 = 4.7V; V_2 = 3V	10			mA	7D
V_{3S}	Output Saturation Voltage	I_3= 15mA; S1 = B V_4 = 4.7V			0.4	V	7D
I_3	Output Leak Current	V3 = 50V; S1 = A			100	µA	7D
V_{4R}	Rising Threshold Voltage	V9 = V_{13}	4.95	5.1	5.25	V	7D
V_{4H}	Hysteresis		0.4	0.5	0.6	V	7D
I_4	Input Bias Current			1	3	µA	7D



TYPICAL PERFORMANCES (using evaluation board) :

n = 83% (V_i = 35V ; V_o = VREF ; I_o = 2A ; f_{sw} = 100KHz)

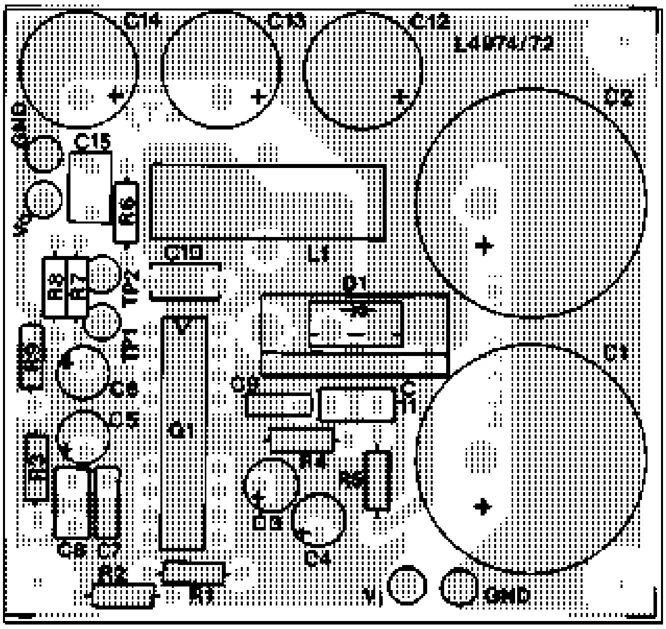
$V_{o\ RIPPLE}$ = 30mV (at 1A)

Line regulation = 12mV (V_i = 15 to 50V)

Load regulation = 7mV (I_o = 0.5 to 2A)

for component values Refer to the fig. 5 (Part list).

Figure 6a : Component Layout of fig.5 (1 : 1 scale). Evaluation Board Available (only for DIP version)



PART LIST

R_1 = 30KΩ
R_2 = 10KΩ
R_3 = 15KΩ
R_4 = 30KΩ
R_5 = 22Ω
R_6 = 4.7KΩ
R_7 = see table A
R_8 = OPTION
R_9 = 4.7KΩ

* C_1 = C_2 = 1000µF 63V EYF (ROE)
C_3 = C_4 = C_5 = C_6 = 2,2µF 50V
C_7 = 390pF Film
C_8 = 22nF MKT 1837 (ERO)
C_9 = 2.7nF KP 1830 (ERO)
C_{10} = 0.33µF Film
C_{11} = 1nF
** C_{12} = C_{13} = C_{14} = 100µF 40V EKR (ROE)
C_{15} = 1µF Film

D1 = SB 560 (OR EQUIVALENT)

L1 = 150µH
core 58310 MAGNETICS
45 TURNS 0.91mm (AWG 19)
COGEMA 949181

* 2 capacitors in parallel to increase input RMS current capability.
* * 3 capacitors in parallel to reduce total output ESR.

Table A

V_0	R_9	R_7
12V	4.7kΩ	6.2kW
15V	4.7kΩ	9.1kΩ
18V	4.7kΩ	12Ω
24V	4.7kΩ	18Ω

Note:
In the Test and Application Circuit for L4972D are not mounted C2, C14 and R8.

Table B
SUGGESTED BOOSTRAP CAPACITORS

Operating Frequency	Boostrap Cap.c10
f = 20KHz	≥680nF
f = 50KHz	≥470nF
f = 100KHz	≥330nF
f = 200KHz	≥220nF
f = 500KHz	≥100nF

Figure 6b: P.C. Board and Component Layout of the Circuit of Fig. 5. (1:1 scale)

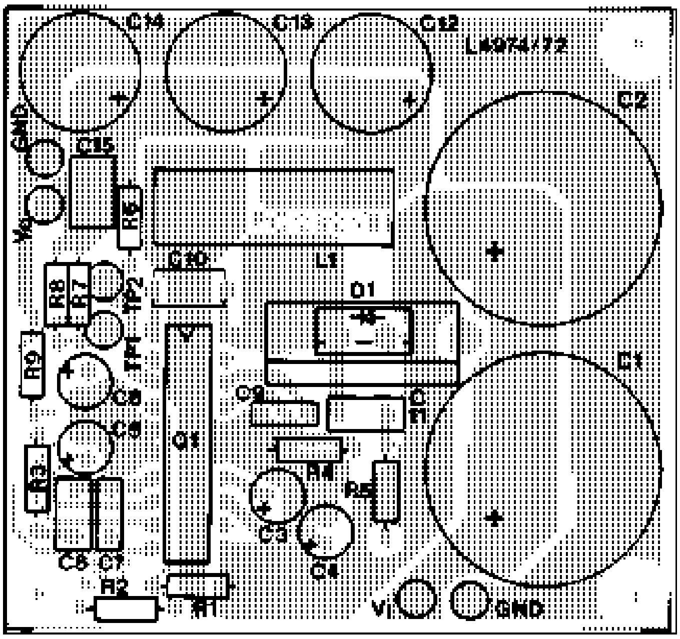


Figure 7 : DC Test Circuits.

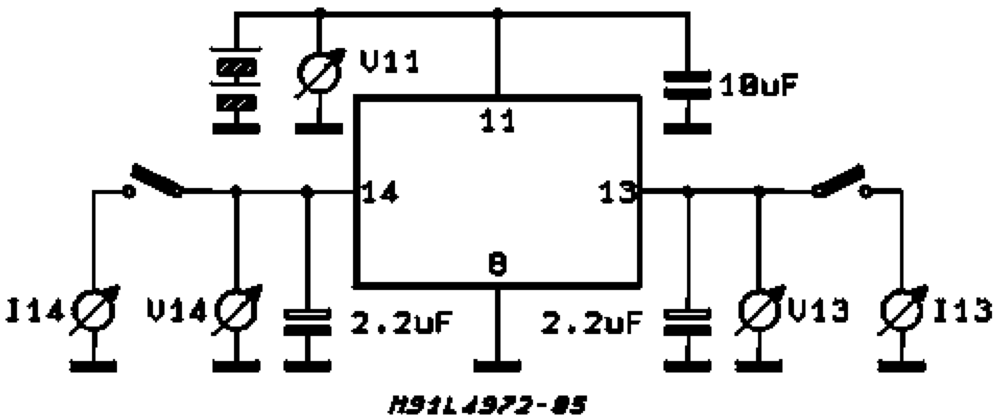


Figure 7A.

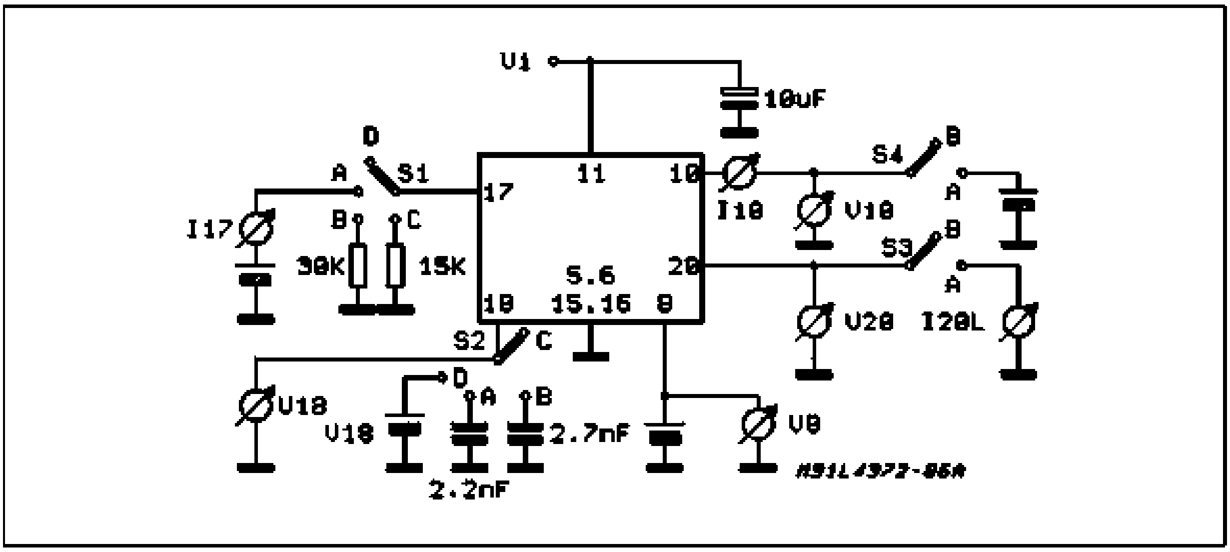


Figure 7B.

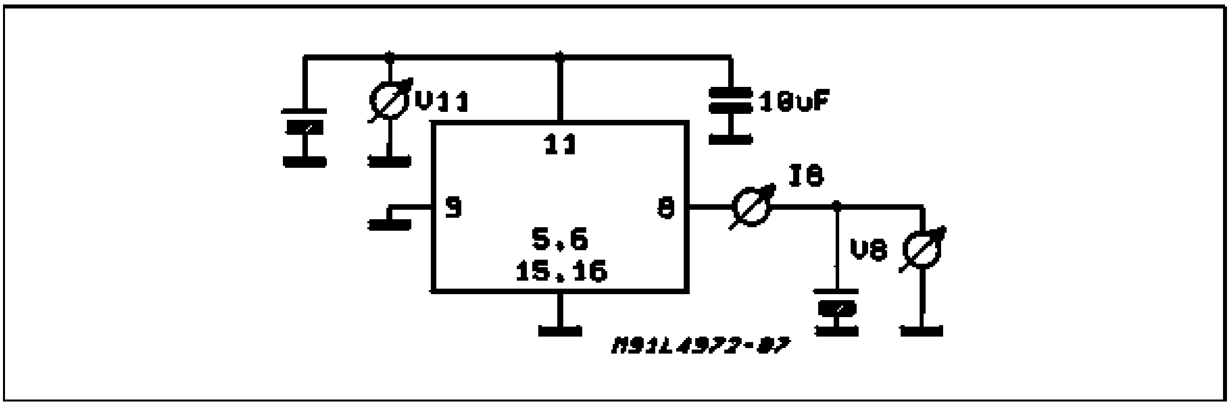


Figure 7C.

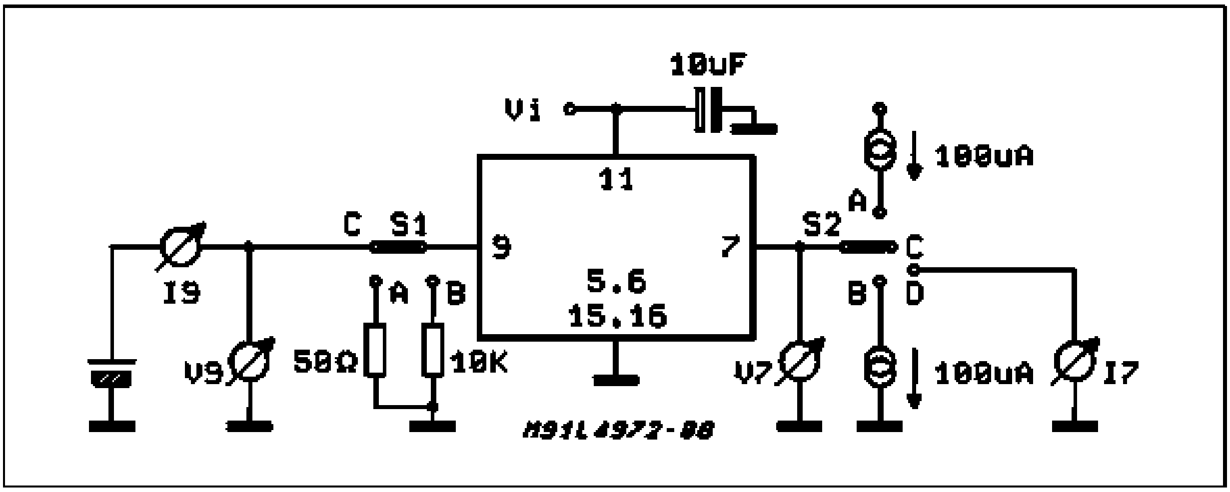


Figure 7D.

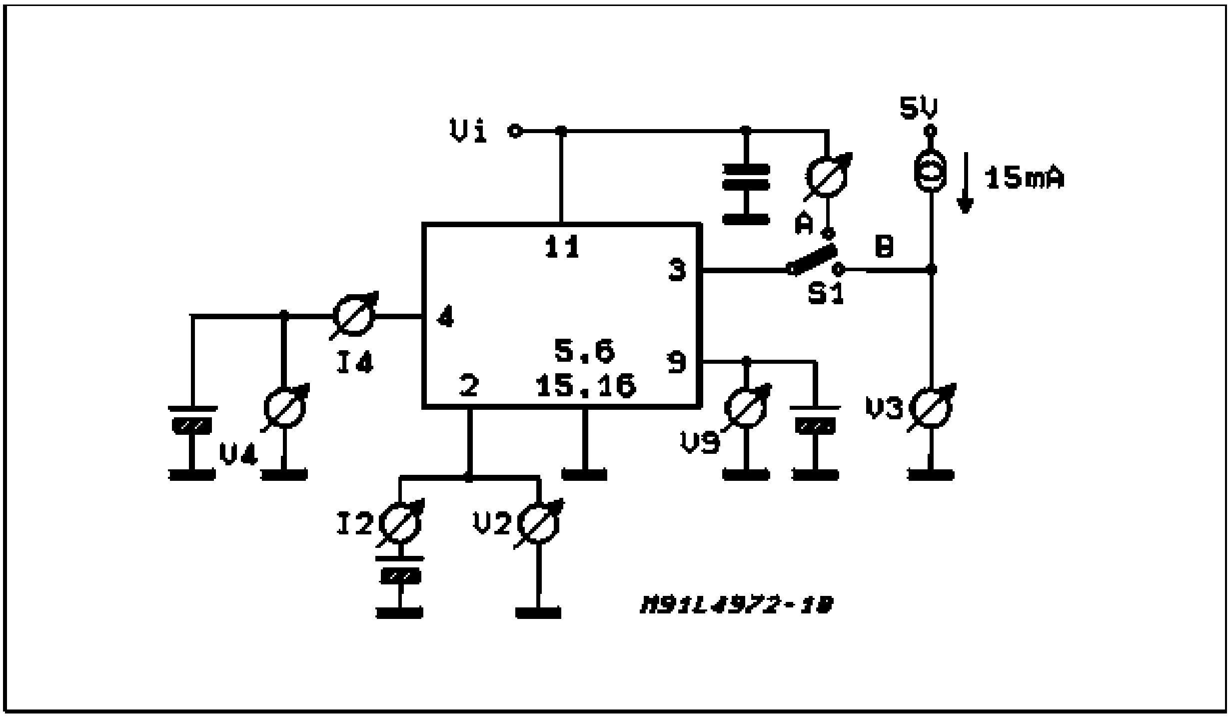


Figure 8 : Quiescent Drain Current vs. Supply Voltage (0% duty cycle - see fig. 7A).

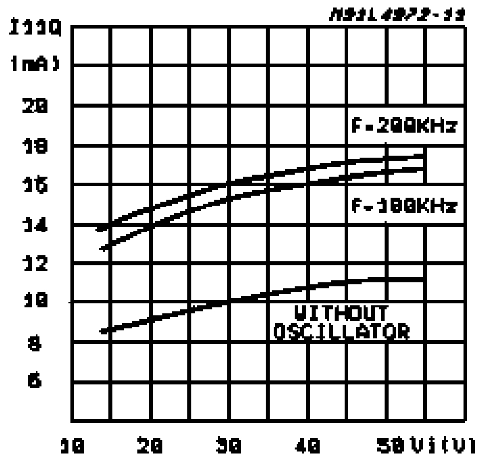


Figure 9 : Quiescent Drain Current vs. Junction Temperature (0% duty cycle).

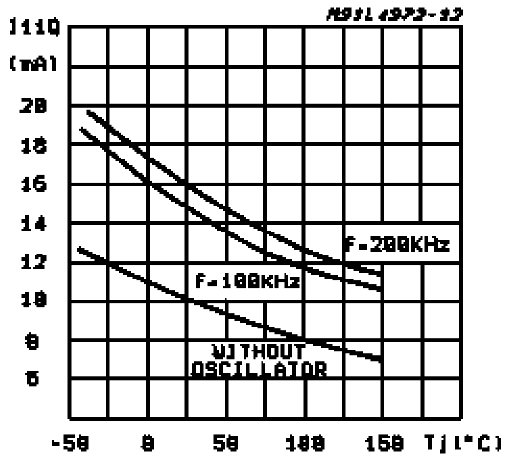


Figure 10 : Quiescent Drain Current vs. Duty Cycle.

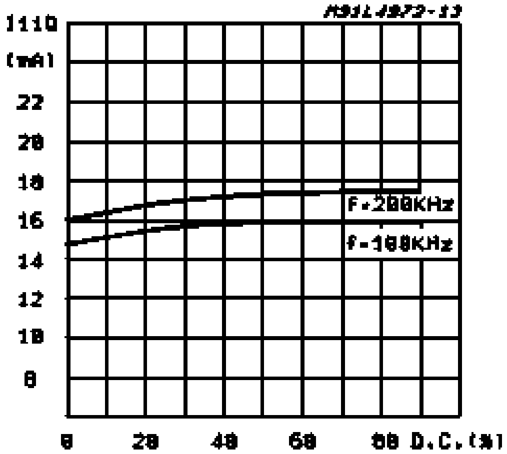


Figure 11 : Reference Voltage (pin 13) vs. Vi (see fig. 7).

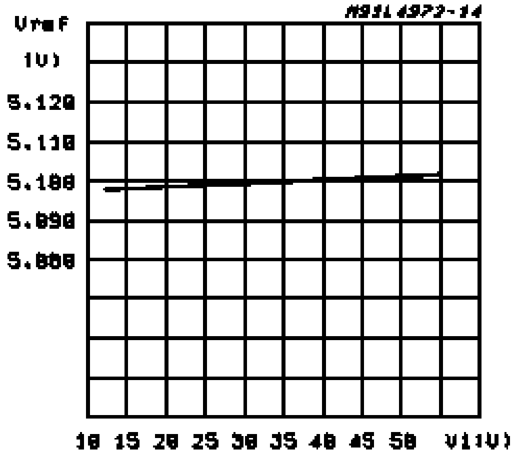


Figure 12 : Reference Voltage (pin 13) vs. Junction Temperature (see fig. 7).

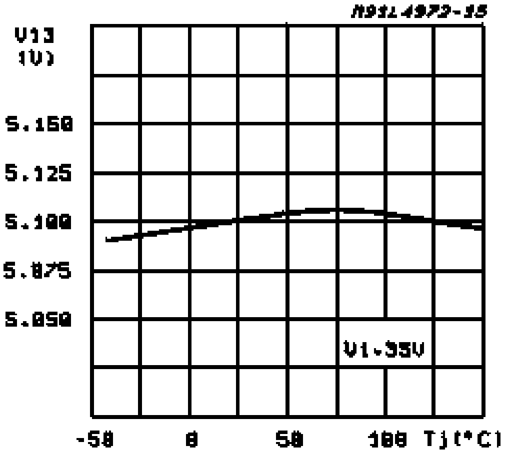


Figure 13 : Reference Voltage (pin 14) vs. Vi (see fig. 7).

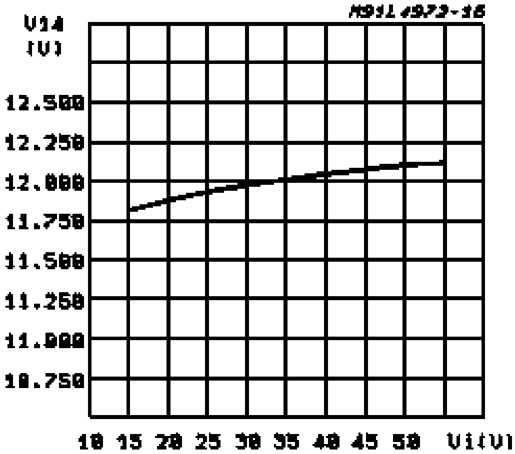


Figure 14 : Reference Voltage (pin 14) vs. Junction Temperature (see fig. 7).

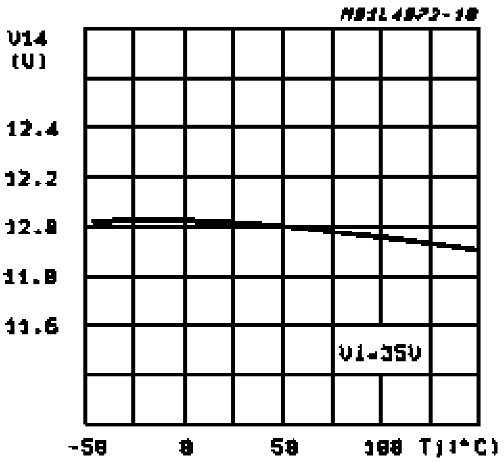
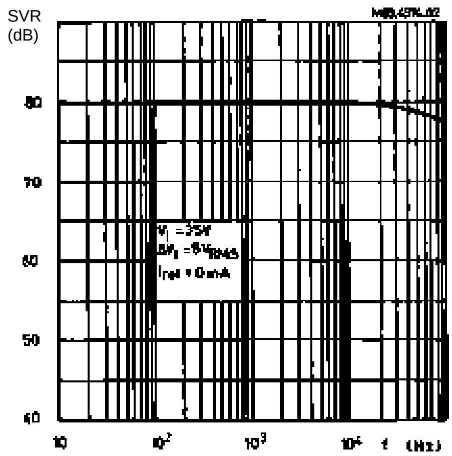


Figure 15 : Reference Voltage 5.1V (pin 13) Supply Voltage Ripple Rejection vs. Fre-



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Figure 16 : Switching Frequency vs. Input Voltage (see fig. 5).

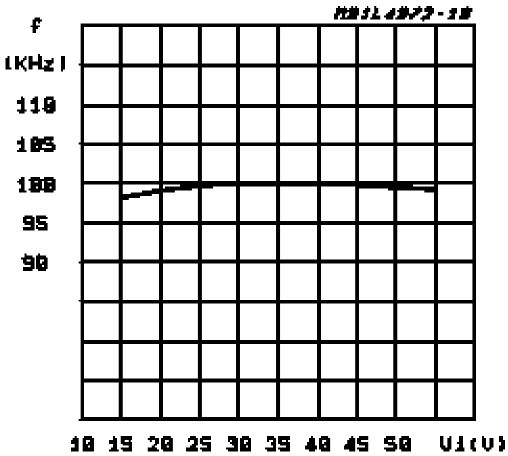


Figure 17 : Switching Frequency vs. Junction Temperature (see fig. 5).

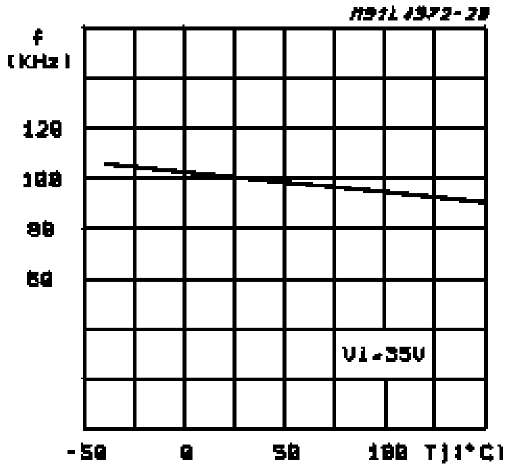


Figure 18 : Switching Frequency vs. R4 (see fig.5).

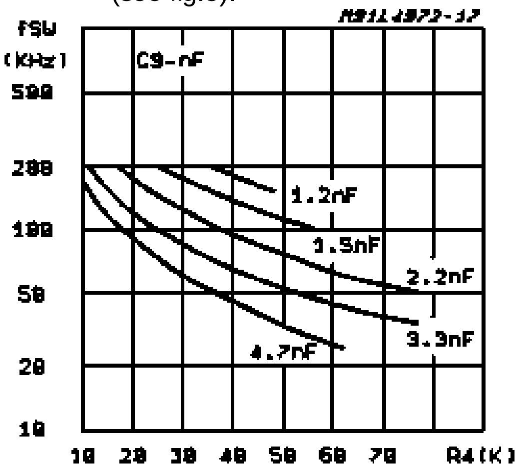


Figure 19 : Maximum Duty Cycle vs. Frequency.

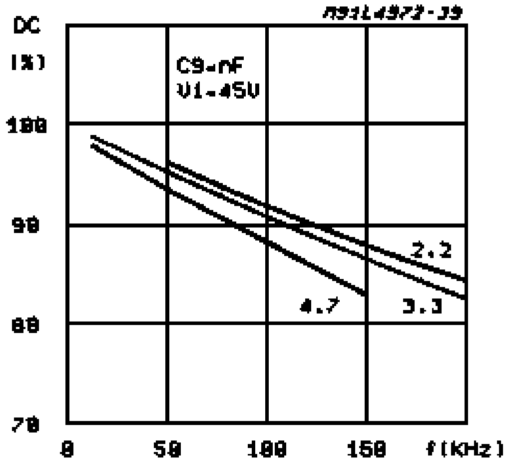


Figure 20 : Supply Voltage Ripple Rejection vs. Frequency (see fig. 5).

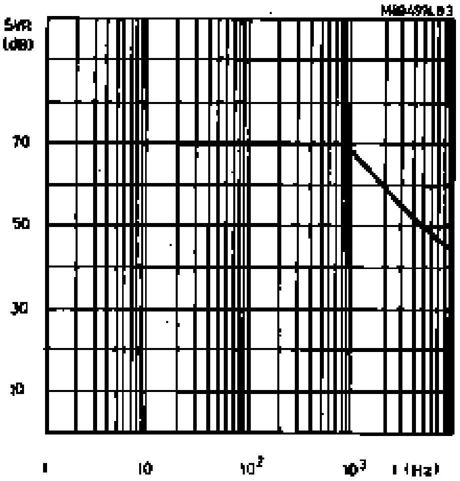


Figure 21 : Efficiency vs. Output Voltage.

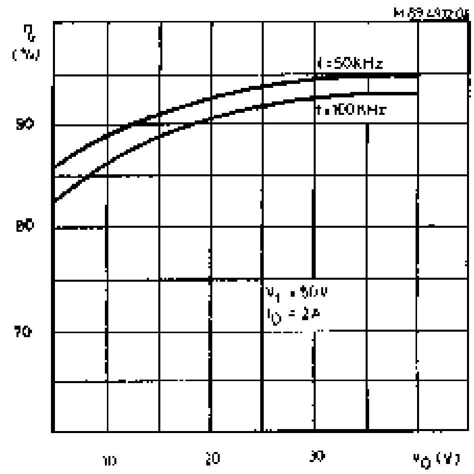


Figure 22 : Line Transient Response (see fig. 5).

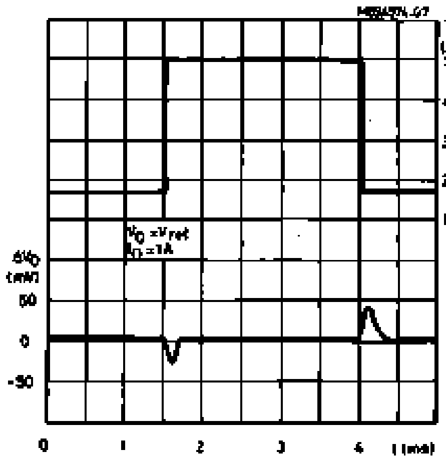


Figure 23 : Load Transient Response (see fig. 5).

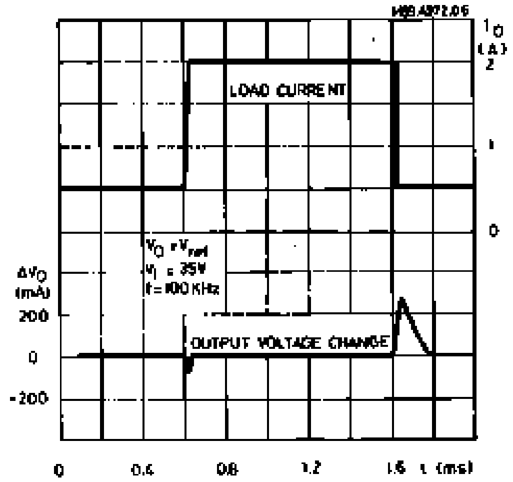


Figure 24 : Dropout Voltage between Pin 11 and Pin 20 vs. Current at Pin 20.

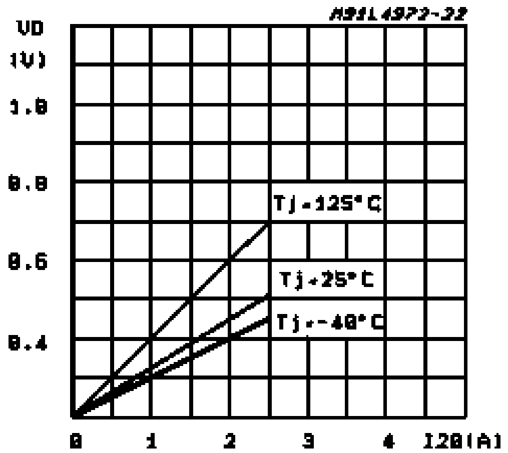


Figure 25 : .Dropout Voltage between Pin 11 and Pin 20 vs. Junction Temperature.

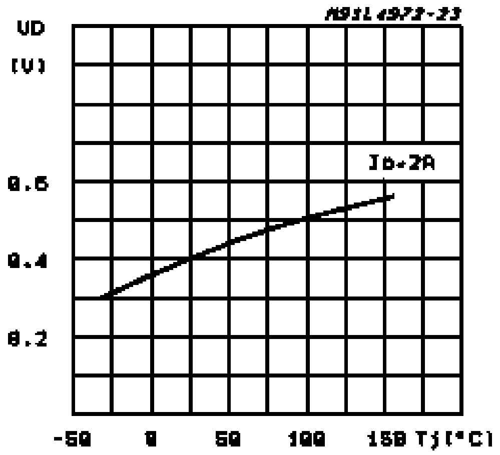


Figure 26 : Power Dissipation (device only) vs. Input Voltage.

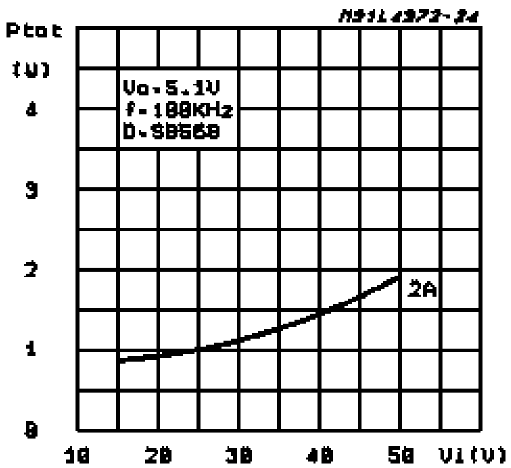


Figure 27 : Power Dissipation (device only) vs. Input Voltage.

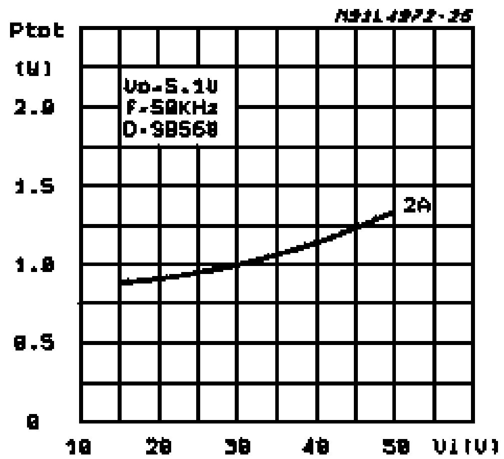


Figure 28 : Power Dissipation (device only) vs. Output Voltage.

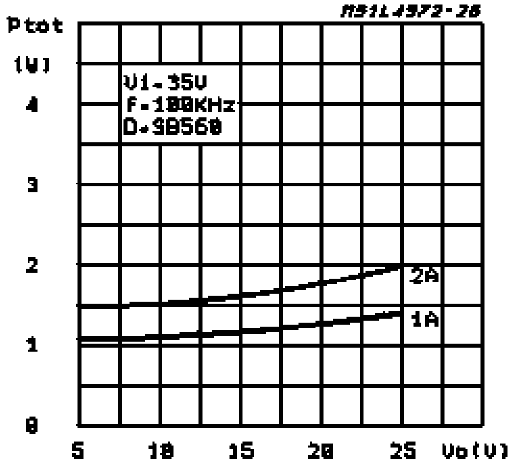


Figure 29 : Power Dissipation (device only) vs. Output Voltage.

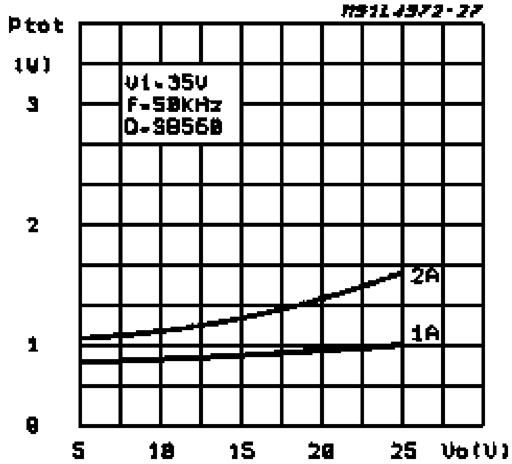


Figure 30 : Power Dissipation (device only) vs. Output Current.

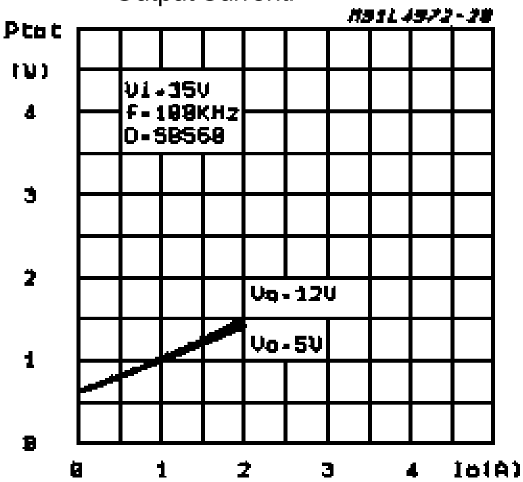


Figure 31 : Power Dissipation (device only) vs. Output Current.

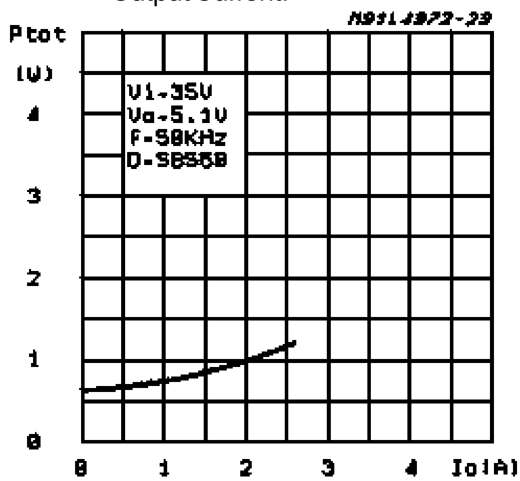


Figure 32 : Efficiency vs. Output Current.

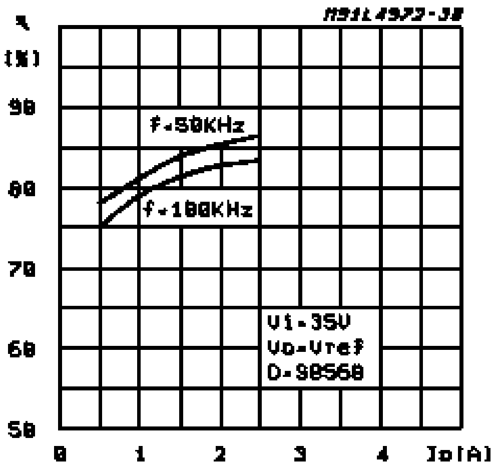


Figure 33 : Test PCB Thermal Characteristic.

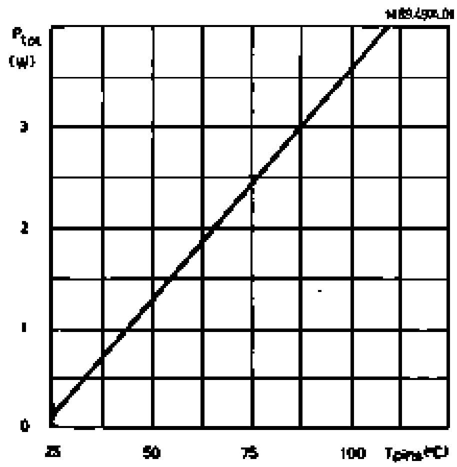


Figure 34 : Junction to Ambient Thermal Resistance vs. Area on Board Heatsink (DIP 16+2+2)

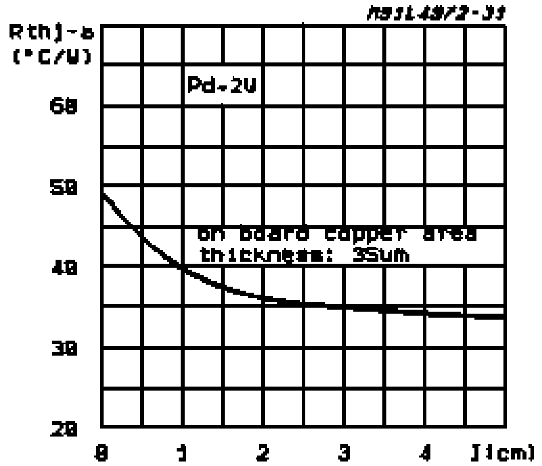


Figure 35: Junction to Ambient Thermal Resistance vs. Area on Board Heatsink (SO20)

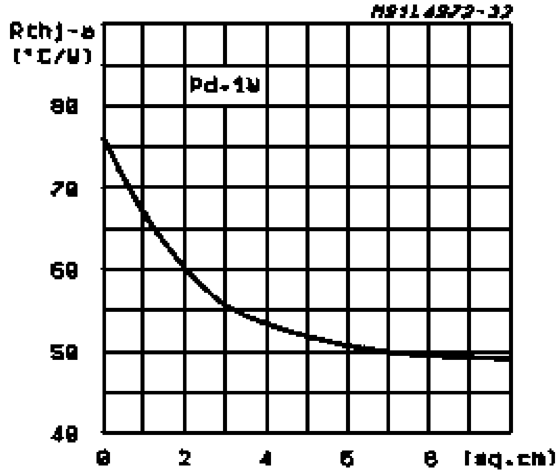


Figure 36: Maximum Allowable Power Dissipation vs. Ambient Temperature (Powerdip)

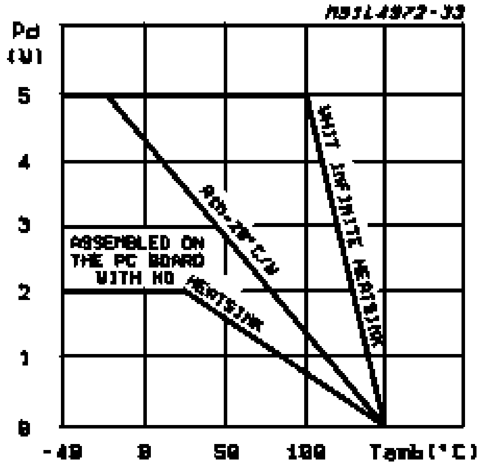


Figure 37: Maximum Allowable Power Dissipation vs. Ambient Temperature (SO20)

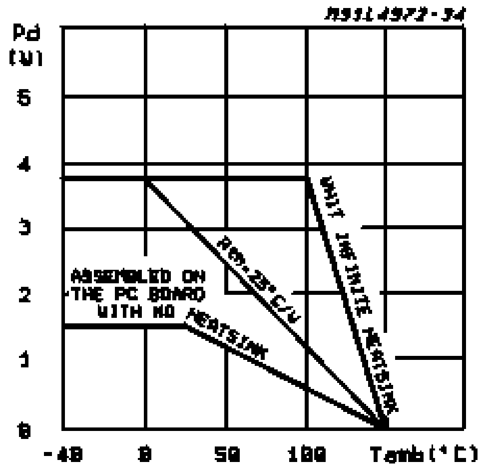


Figure 38: Open Loop Frequency and Phase of Error Amplifier (see fig. 7C).

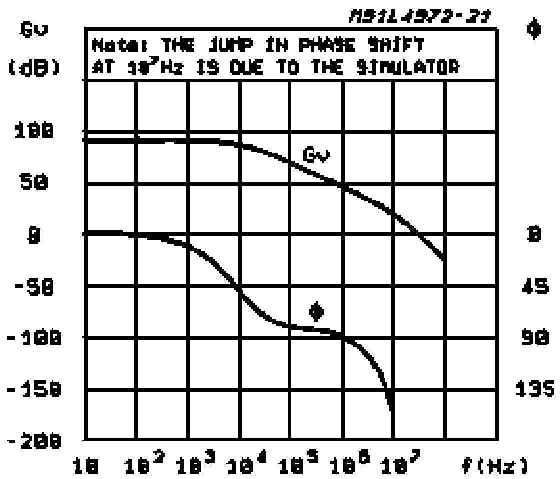


Figure 39 : 2A – 5.1V Low Cost Application Circuit.

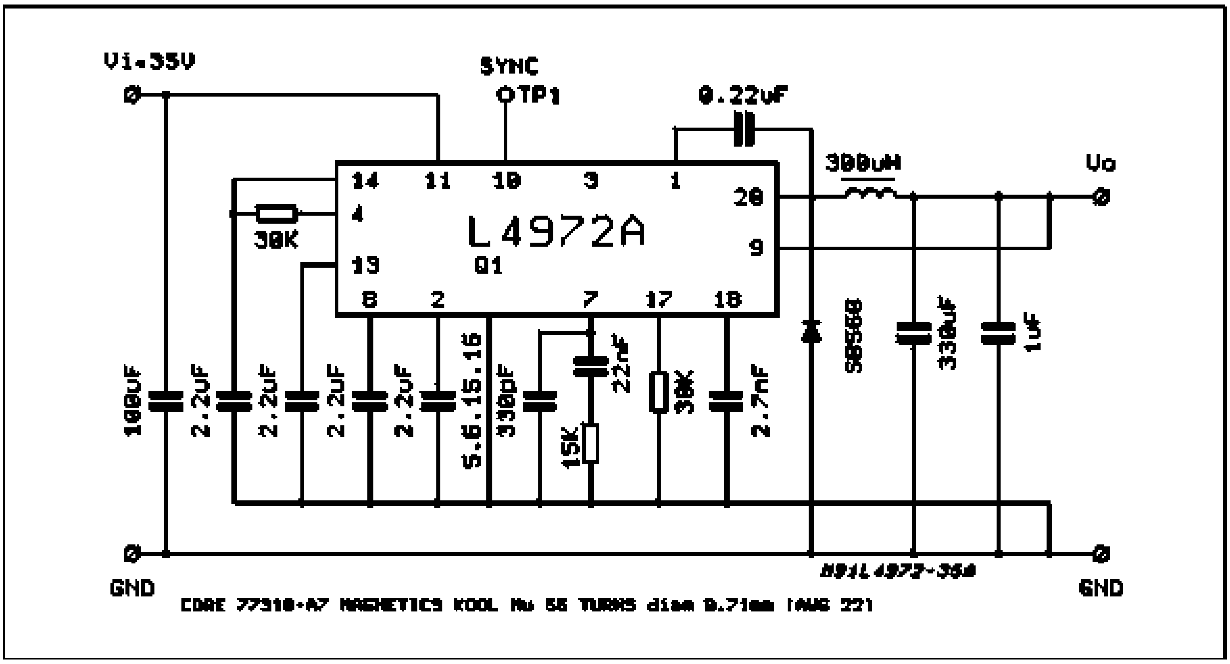


Figure 40 : A 5.1V/12V Multiple Supply. Note the Synchronization between the L4972A and L4970A.

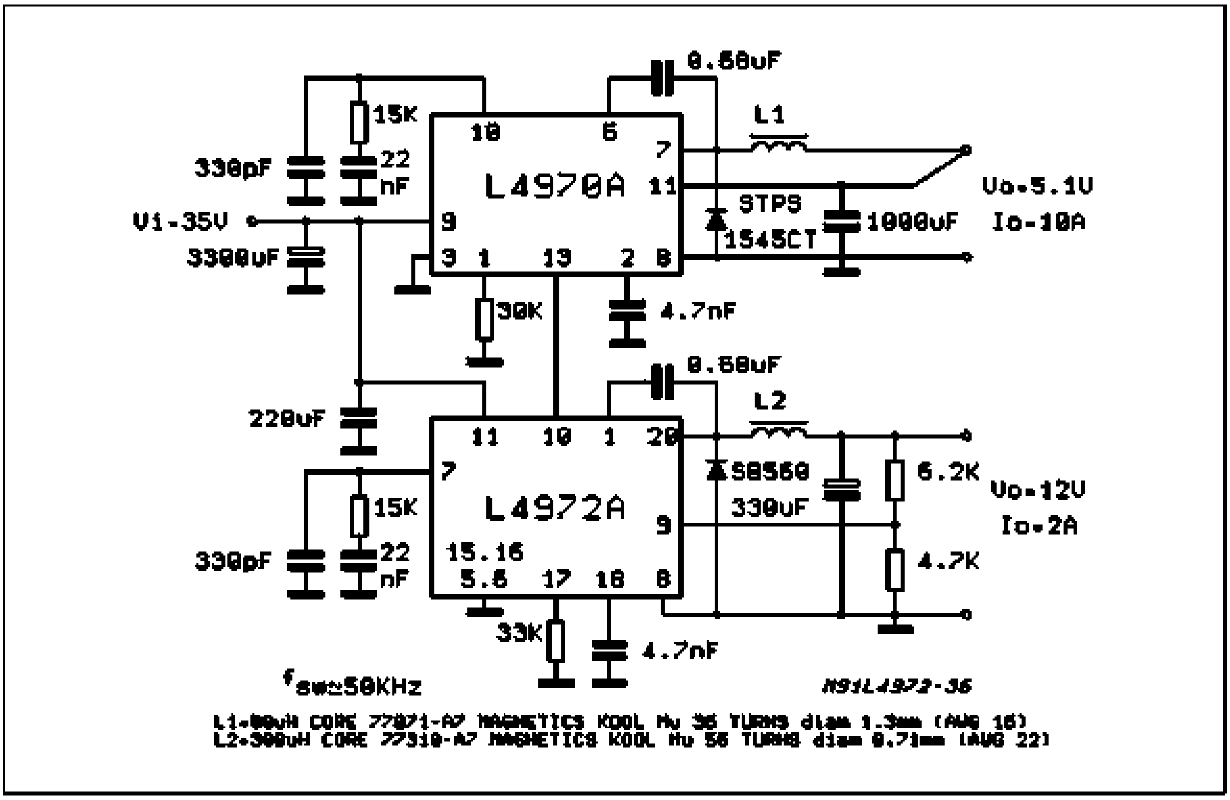


Figure 41 : L4972A's Sync. Example.

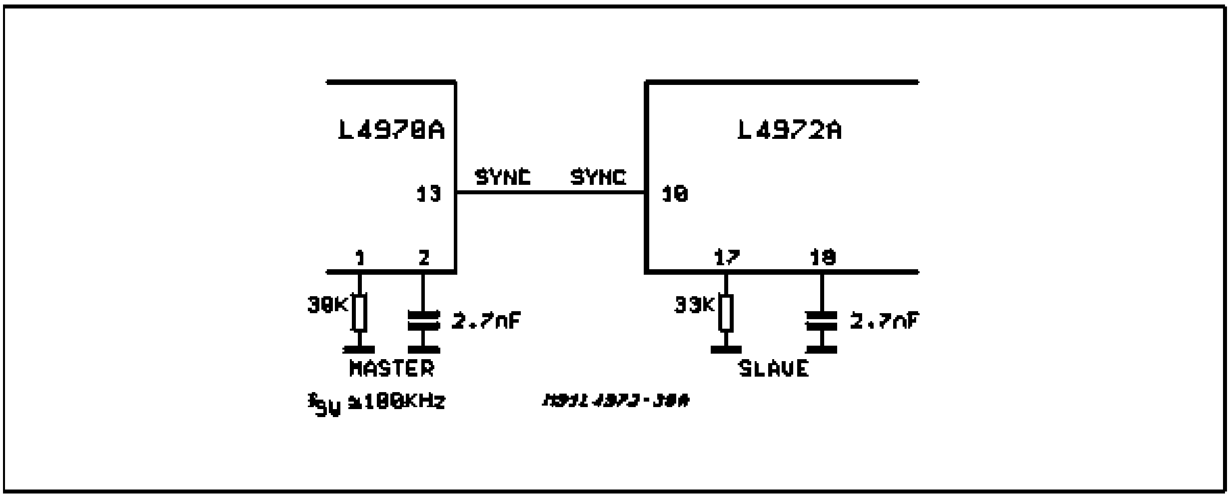
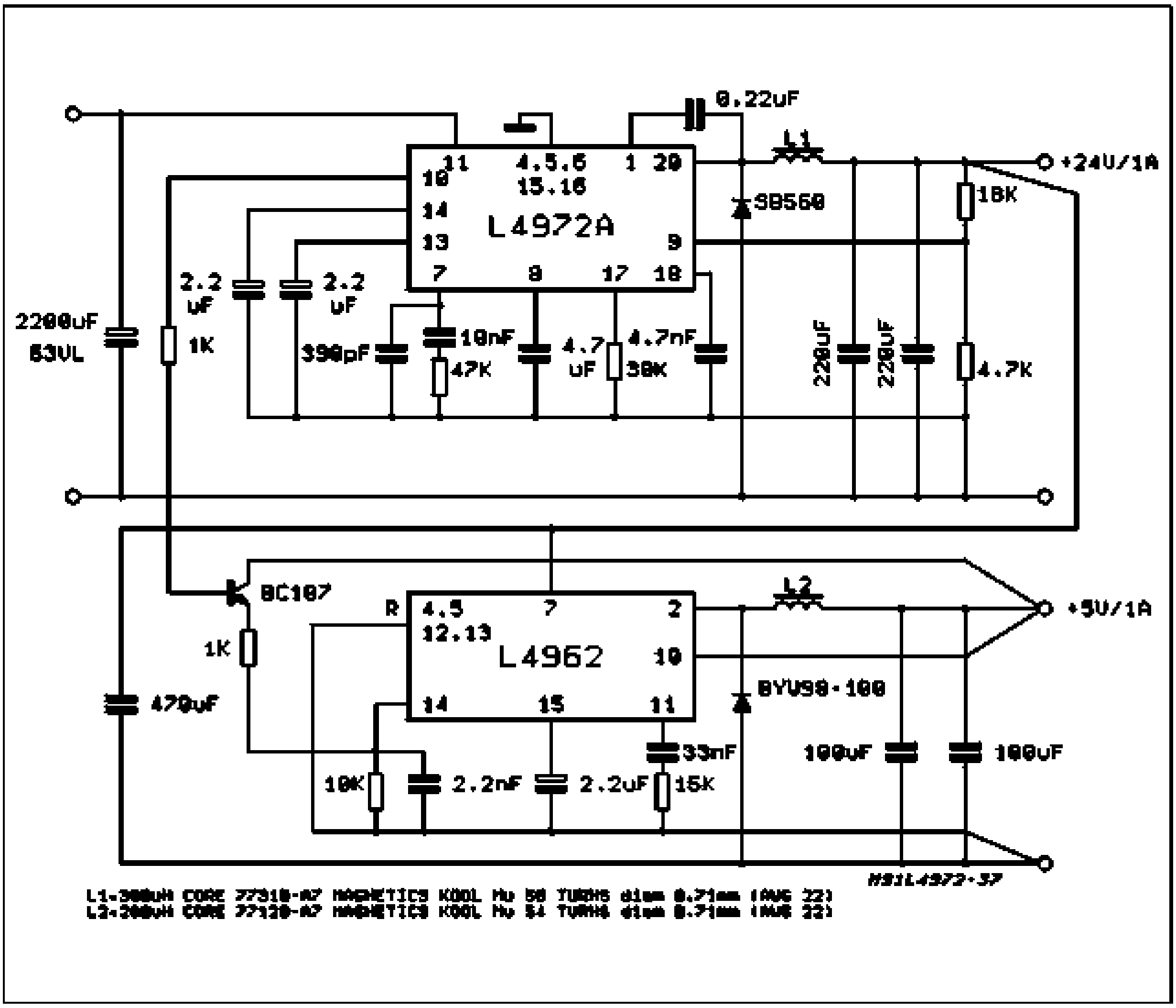
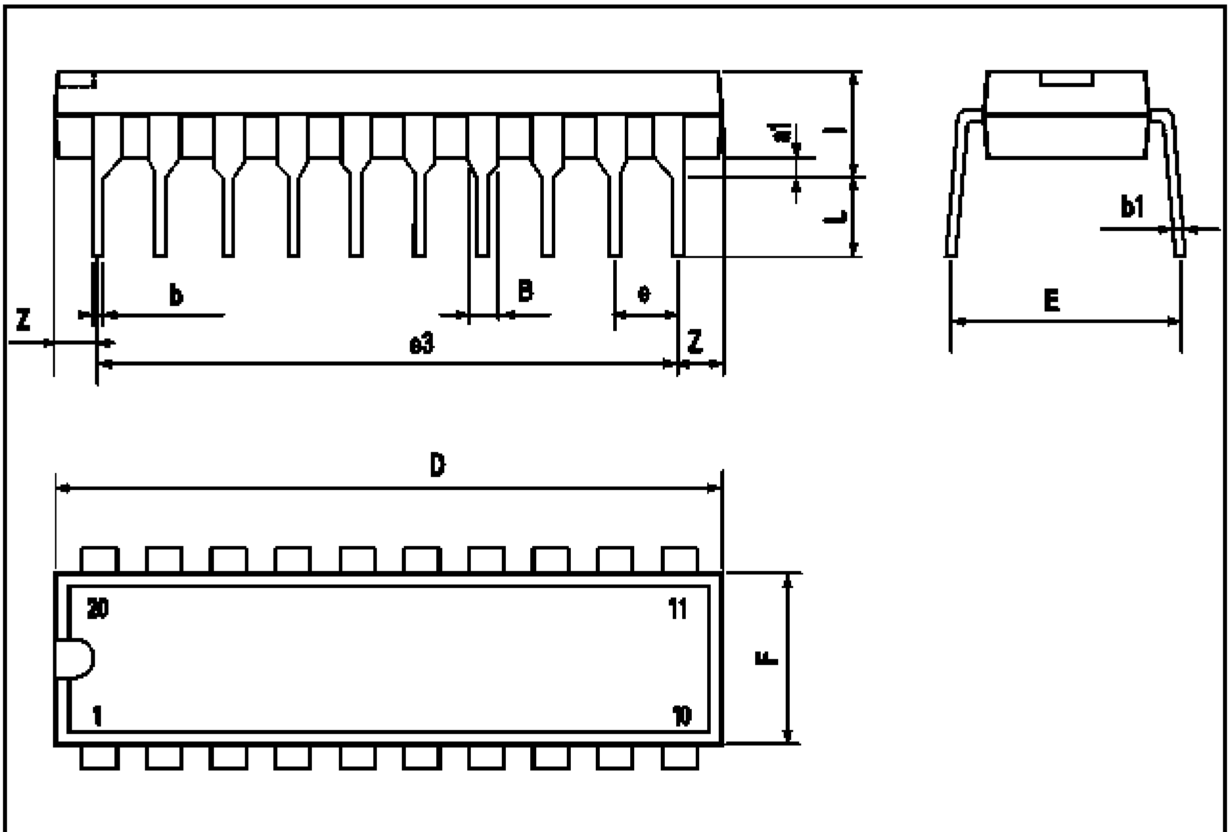


Figure 42: 1A/24V Multiple Supply. Note the synchronization between the L4972A and L4962



POWERDIP20 PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.85		1.40	0.033		0.055
b		0.50			0.020	
b1	0.38		0.50	0.015		0.020
D			24.80			0.976
E		8.80			0.346	
e		2.54			0.100	
e3		22.86			0.900	
F			7.10			0.280
I			5.10			0.201
L		3.30			0.130	
Z			1.27			0.050



SO20 PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.1		0.3	0.004		0.012
a2			2.45			0.096
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.013
C		0.5			0.020	
c1	45 (typ.)					
D	12.6		13.0	0.496		0.512
E	10		10.65	0.394		0.419
e		1.27			0.050	
e3		11.43			0.450	
F	7.4		7.6	0.291		0.299
L	0.5		1.27	0.020		0.050
M			0.75			0.030
S	8 (max.)					

